Electronic Version
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Claims

[c1] 1.A method for small signal sensing during a read operation of a static random access memory (SRAM) cell, the method comprising:
coupling a pair of complementary sense amplifier data lines to a corresponding pair of complementary bit lines associated with the SRAM cell; and
setting a sense amplifier so as to amplify a signal developed on said sense amplifier data lines;
wherein said bit line pair remains coupled to said sense amplifier data lines at the time said sense amplifier is set.

[c2] 2.The method of claim 1, further comprising clamping one of said pair of complementary sense amplifier data lines to a logic high voltage upon activation of a word line associated with the SRAM cell.

[c3] 3.The method of claim 2, wherein said clamping to said logic high voltage is implemented through configuring the SRAM cell with PFET access transistors.

[c4] 4.The method of claim 3, wherein said clamping is implemented through one of a pair of pull up transistors

within the SRAM cell.

[c5] 5.The method of claim 4, wherein said pair of pull up transistors within the SRAM cell has larger a pull up strength relative to a pull down strength of a pair of pull down transistors within the SRAM cell.

[c6] 6.The method of claim 1, wherein said pair of complementary sense amplifier data lines is coupled to said corresponding pair of complementary bit lines through a pair of activated bit switches.

[c7] 7.A method for implementing a read operation for a static random access memory (SRAM) cell, the method comprising:
activating a word line associated with the SRAM cell;
deactivating a precharge circuit configured for precharging a pair of complementary bit lines associated with the SRAM cell;
coupling a corresponding pair of complementary sense amplifier data lines to said pair of complementary bit lines associated with the SRAM cell; and
setting a sense amplifier so as to amplify a signal developed on said sense amplifier data lines;
wherein said bit line pair remains coupled to said sense amplifier data lines at the time said sense amplifier is set.

[c8] 8.The method of claim 7, further comprising clamping one of said pair of complementary sense amplifier data lines to a logic high voltage upon activation of a word line associated with the SRAM cell.

[c9] 9.The method of claim 8, wherein said clamping to said logic high voltage is implemented through configuring the SRAM cell with PFET access transistors.

[c10] 10.The method of claim 9, wherein said clamping is implemented through one of a pair of pull up transistors within the SRAM cell.

[c11] 11.The method of claim 10, wherein said pair of pull up transistors within the SRAM cell has larger a pull up strength relative to a pull down strength of a pair of pull down transistors within the SRAM cell.

[c12] 12.The method of claim 7, wherein said pair of complementary sense amplifier data lines is coupled to said corresponding pair of complementary bit lines through a pair of activated bit switches.

[c13] 13.An apparatus for small signal sensing during a read operation of a static random access memory (SRAM) cell, comprising:

a pair of complementary sense amplifier data lines selec-

tively coupled to a corresponding pair of complementary bit lines associated with the SRAM cell; and
a sense amplifier configured to amplify a signal developed on said sense amplifier data lines;
wherein said bit line pair is coupled to said sense amplifier data lines whenever said sense amplifier is set.

[c14] 14.The apparatus of claim 13, wherein one of said pair of complementary sense amplifier data lines is configured to be clamped to a logic high voltage upon activation of a word line associated with the SRAM cell.

[c15] 15.The apparatus of claim 14, further comprising a pair of PFET access transistors associated with the SRAM cell, said PFET access transistors configured to clamp said pair of complementary sense amplifier data lines to said logic high voltage

[c16] 16.The apparatus of claim 15, wherein said clamp is further implemented through one of a pair of pull up transistors within the SRAM cell.

[c17] 17.The apparatus of claim 16, wherein said pair of pull up transistors within the SRAM cell has larger a pull up strength relative to a pull down strength of a pair of pull down transistors within the SRAM cell.

[c18] 18.The apparatus of claim 13, wherein said pair of com-

plementary sense amplifier data lines is coupled to said corresponding pair of complementary bit lines through a pair of activated bit switches.